The SIGMA Project

The SIGMA Architecture

- RISC based architecture
- 128 Bit
- 32 General Purpose registers
- 32 Floating Point registers
- 32 SIMD registers (256 bit)
- Up to quad precision floating point
- SIMD functionality
- Little endian

Why Make a New ISA?

- Because we can
- Many modern day architectures still contain legacy instructions, compatibility modes, etc. that increase complexity and die sizes.
- ARM and x86, the most common high-performance ISAs have legally restricting licenses.
- Existing open source ISAs are outdated and mostly abandoned, with the exception of RISC-V
- RISC-V was originally conceived for educational purposes, not commercial usage; it is also incomplete as an architecture in many aspects, such as the lack of a ratified memory model or any SIMD instructions

Electron Microarchitecture

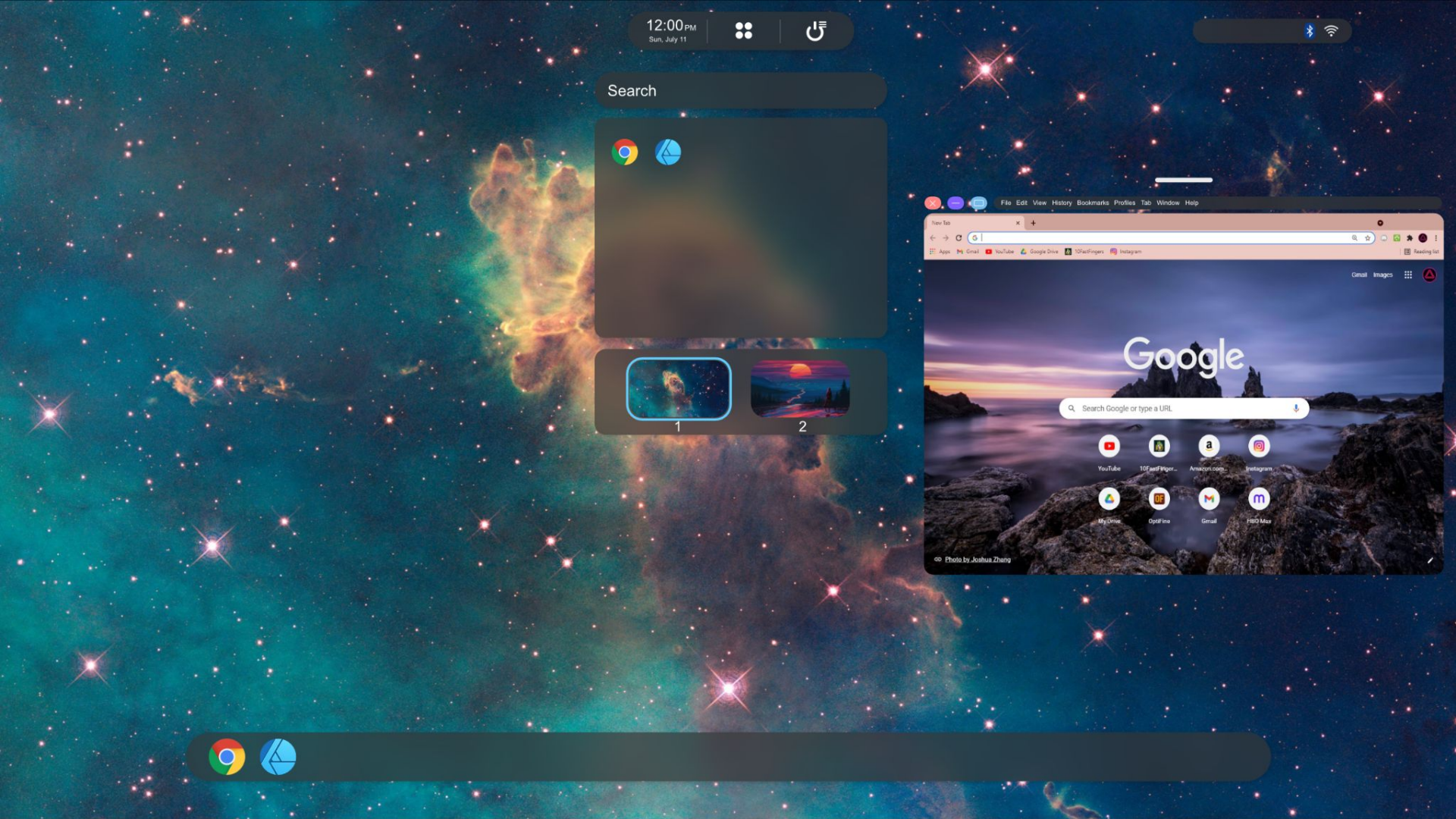
- ~10 stage pipeline with 6 decode stages
- 6 - 10 ALUs
- Capable of simultaneous multithreading
- 2-4 Floating point units
- 2-4 SIMD units

North Star SOC

- 30 PCIe 4.0 lanes
- 20 USB 4 lanes
- DDR5 memory controller
- 512K L1 cache
- 10MB L2 cache total
- Direct VRAM write-only interface for GPU

The Nebula Operating System

- Clean UI
- Personalization options
- Based on linux
- Ported GCC compiler
- New package manager
- ZSH shell
- Tarball build commands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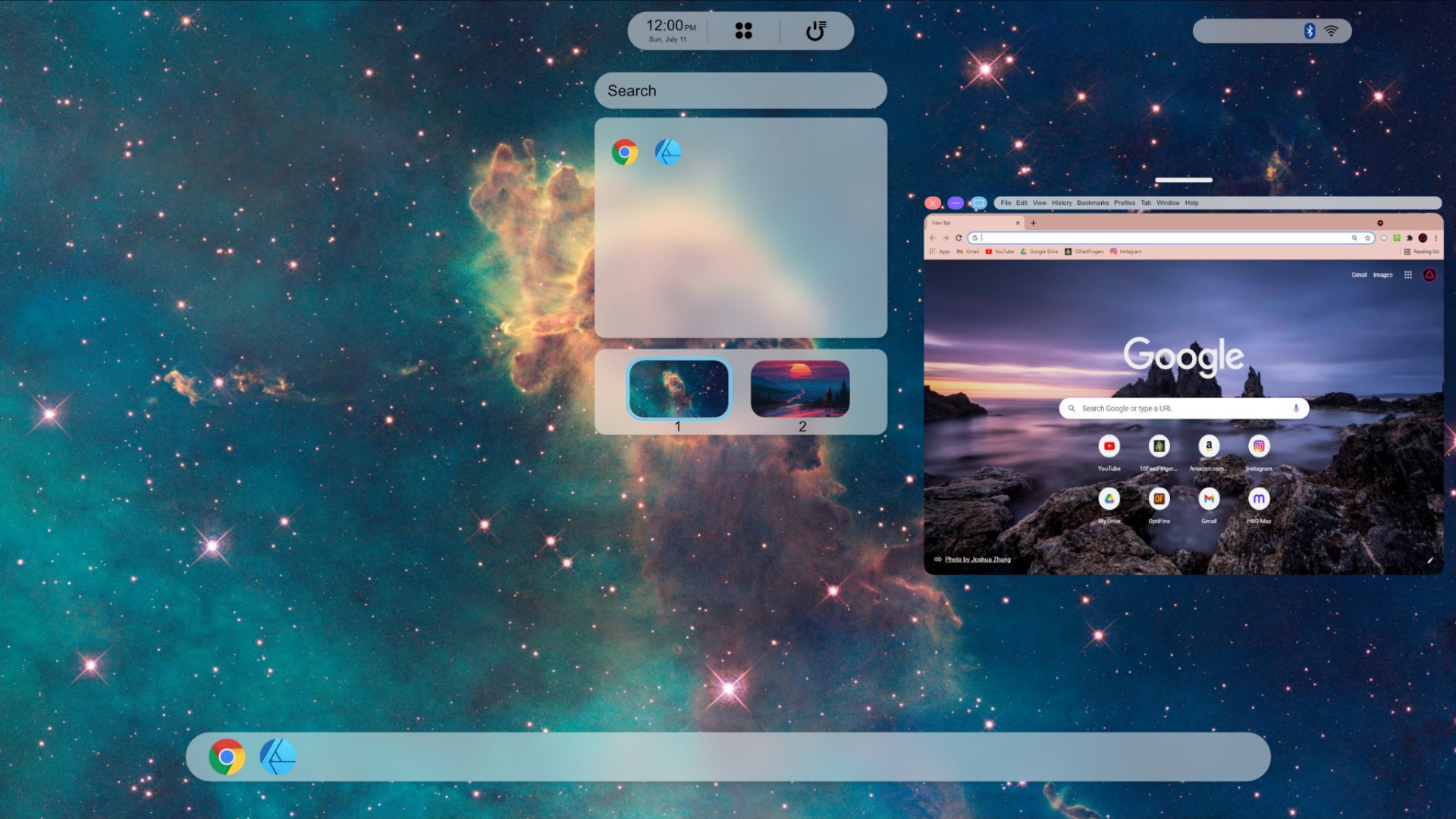
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